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10/721,178	11/26/2003	Shih-Lien L. Lu	INTEL-0034	6618

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EXAMINER	
KIM, DANIEL Y	
ART UNIT	PAPER NUMBER
2185	

DATE MAILED: 10/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/721,178	LU ET AL.	
	Examiner	Art Unit	
	Daniel Kim	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 September 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *6-25,27,28,30,32-37,39 and 40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *6-25,27,28,30,32-37,39 and 40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 November 2005 and 26 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This Office Action is in response to applicant's communication filed September 19, 2006 in response to the PTO Office Action mailed July 26, 2006. The applicant's remarks and amendments to the claims and/or the specification were considered with the results that follow.

2. In response to the last Office Action, claims 6, 16, 19, 25, 27, 32-33, 35 and 40 have been amended, claims 29, 31 and 38 have canceled and no claims have been added. Claims 6-25, 27-28, 30, 32-37 and 39-40 remain pending in this application.

3. Applicant's request for reconsideration of the finality of the rejection of the last Office action is persuasive and, therefore, the finality of that action is withdrawn.

Response to Arguments

4. Applicant's arguments filed September 7, 2006, with respect to the rejection(s) of claim(s) 6-15, 18, 20, 25, 27-28, 31, 33-37 under 35 U.S.C. 103(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of the following:

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 6-9, 14-17, 19-20, 25, 27-28, 32-37 and 40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miller (US PGPub No. 20040100994), Bhattacharya et al (US Patent No. 7,047,385) and Berg et al (US Patent No. 6,732,247).

For claim 6, Miller discloses a memory comprising:

a plurality of systolic memory arrays (systolic memory arrays that grow in size as the number of inputs grow, par. 0035).

Miller fails to disclose each array is divided into banks, each of the memory arrays arranged in a pipelined architecture and each of the plurality of memory arrays to support pipeline access to the corresponding banks using a plurality of data pipes.

Bhattacharya helps disclose multiple arrays of memory banks (col. 3, lines 35-36), and addresses input from an address interface by an address pipeline and data read from memory blocks to a data out interface by a data pipeline (col. 1, lines 51-54).

These teachings fail to disclose a plurality of pipeline registers, each register to couple to one end of a corresponding one of the plurality of systolic memory arrays.

Berg helps disclose memory banks are connected in pipelined fashion to pipeline registers placed at regular intervals on a global bus (col. 2, lines 18-20).

It would have been obvious to a person of ordinary skill in the art at the time of the invention to combine Miller, Bhattacharya and Berg to include pipeline registers because this would allow wire lengths to be kept short (col. 2, lines 20-21), as taught by Berg.

For claim 7, the combined teachings of Miller, Bhattacharya and Berg as per rejection of claim 6 above further help disclose at least one of the plurality of data pipes is used for a reading operation (Berg: the multi-ported pipelined memory performs read and write operations on a shared data bus of a read write port simultaneously, col. 2, lines 27-29).

For claim 8, the combined teachings of Miller, Bhattacharya and Berg as per rejection of claim 6 above further help disclose at least one of the plurality of data pipes is used for a writing operation (Berg: col. 2, lines 27-29).

For claim 9, the combined teachings of Miller, Bhattacharya and Berg as per rejection of claim 6 above further help disclose each of the plurality of systolic memory arrays includes at least eight banks (Bhattacharya: fig. 1a, MB1 to $MB2^N$).

For claim 14, the combined teachings of Miller, Bhattacharya and Berg as per rejection of claim 6 further help disclose each of the plurality of systolic memory arrays is divided into a horizontal arrangement (Miller: memories are connected in a matrix to form a systolic memory array, par. 0038; a systolic array having memories connected in a nearest-neighbor fashion to allow the connection of any input to any output by the last column, par. 0037).

For claim 15, the combined teachings of Miller, Bhattacharya and Berg as per rejection of claim 6 further help disclose each of the plurality of systolic memory arrays is divided into a vertical arrangement (Miller: par. 0038; a number of column storage memory devices required to implement these systolic arrays, par. 0008).

For claim 16, the combined teachings of Miller, Bhattacharya and Berg as per rejection of claim 6 are incorporated herein.

These teachings further help disclose a memory comprising:

a plurality of systolic memory arrays (Miller: par. 0035) each of the memory arrays arranged in a pipelined architecture and each of the plurality of memory arrays to support pipeline access to the corresponding banks using a plurality of data pipes (Bhattacharya: col. 3, lines 35-36; col. 1, lines 51-54), wherein a writing operation into the memory is performed by pumping an address with data that is to be written into the memory (Berg: a request is processed in pipelined fashion over multiple clock cycles, the ensuring access requests also may be either read access requests or write access requests, col. 2, lines 46-48).

For claim 17, the combined teachings of Miller, Bhattacharya and Berg as per rejection of claim 6 further help disclose a read operation from memory is performed by pumping an address once and allowing the address to flow through an address pipe to reach individual banks of one of the systolic memory arrays one cycle at a time (Berg: col. 2, lines 46-48).

For claim 19, the combined teachings of Miller, Bhattacharya and Berg as per rejection of claim 16 further help disclose peripheral access for one systolic memory

array is accomplished from one side of the one systolic memory array (Berg: one or more peripheral devices, col. 3, lines 25-26; col. 2, lines 18-20).

For claim 20, the combined teachings of Miller, Bhattacharya and Berg as per rejection of claim 6 further help disclose whenever a bank receives a read address, memory access is initiated (Berg: col. 2, lines 46-48).

For claim 25, the combined teachings of Miller, Bhattacharya and Berg as per rejection of claim 6 are incorporated herein.

These teachings further help disclose a processing system comprising:

a die including a microprocessor (Berg: a processor die serving as an addressable on-chip memory, col. 1, line 67; col. 2, line 1);

peripheral equipment coupled to the processing system (Berg: the computing system also includes a display, one or more input devices, one or more peripheral devices, col. 3, lines 23-31);

a network interface (Berg: computing system with pipelined data banks may include a communication or network interface, col. 3, lines 32-34); and

on-die or off-die systolic memory (Berg: a multi-ported pipelined memory that is located on a processor die serving as an addressable on-chip memory, col. 1, lines 66-67, col. 2, line 1), the systolic memory including:

a plurality of separate systolic memory arrays, each memory array including a plurality of memory banks in a pipelined fashion, the plurality of memory banks of each memory array to share an address line in a pipelined fashion and data lines in a pipelined fashion (Miller: par. 0035; Battacharya: col. 3, lines 35-36; col. 1, lines 51-54;

Berg: col. 2, lines 27-29; a data request is made by providing an address on the address inputs and asserting the read signal, col. 4, lines 44-46).

For claim 27, the combined teachings of Miller, Bhattacharya and Berg as per rejection of claim 25 further help disclose the system memory further includes a plurality of pipeline registers, each register coupled to one of the separate systolic memory arrays (Berg: col. 2, lines 18-20).

For claim 28, the combined teachings of Miller, Bhattacharya and Berg as per rejection of claim 25 further help disclose each bank is associated with a mechanism to support addressing and data operations (Bhattacharya: addresses input from an address interface of the IC supplies to the memory blocks by an address pipeline and data read from the memory blocks supplied to a data out interface of the IC by a data pipeline, col. 1, lines 51-54).

For claim 32, the combined teachings of Miller, Bhattacharya and Berg as per rejection of claim 27 further help disclose each register is coupled to one end of a corresponding one of the systolic memory arrays (Berg: col. 2, lines 18-20).

For claim 33, the combined teachings of Miller, Bhattacharya and Berg as per rejection of claim 6 further help disclose each register is coupled to a first one of the banks arranged in the pipelined architecture of a corresponding one of the memory arrays (Berg: col. 2, lines 18-20).

For claim 34, the combined teachings of Miller, Bhattacharya and Berg as per rejection of claim 6 further help disclose each bank is associated with a mechanism to

support addressing each data operation of the corresponding bank (Bhattacharya: col. 1, lines 51-54).

For claim 35, the combined teachings of Miller, Bhattacharya and Berg as per rejection of claim 6 are incorporated herein.

These teachings further help disclose a memory comprising:

a plurality of separate systolic memory arrays (Miller: par. 0035) each memory array including a plurality of memory banks in pipelined fashion, the plurality of memory banks of each memory array to share an address line in a pipelined fashion and data lines in a pipelined fashion (Bhattacharya: col. 3, lines 35-36; col. 1, lines 51-54), wherein a read operation is performed by pumping an address and allowing the address to flow through the address line to reach individual banks of one of the plurality of separate systolic memory arrays one cycle at a time (Berg: col. 2, lines 46-48).

For claim 36, the combined teachings of Miller, Bhattacharya and Berg as per rejection of claim 35 further help disclose a plurality of pipeline registers, each register to couple to one of the separate systolic memory arrays (Berg: col. 2, lines 18-20).

For claim 37, the combined teachings of Miller, Bhattacharya and Berg as per rejection of claim 35 further help disclose each bank is associated with a mechanism to support addressing and data operations (Bhattacharya: col. 1, lines 51-54).

For claim 40, the combined teachings of Miller, Bhattacharya and Berg as per rejection of claim 6 are incorporated herein.

These teachings further help disclose a plurality of separate systolic memory arrays (Miller: par. 0035) each memory array including a plurality of memory banks in pipelined

fashion, the plurality of memory banks of each memory array to share an address line in a pipelined fashion and data lines in a pipelined fashion (Bhattacharya: col. 3, lines 35-36; col. 1, lines 51-54), wherein peripheral access for one systolic memory array is accomplished from one side of the one systolic memory array (Berg: col. 3, lines 25-26; col. 2, lines 18-20).

7. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Miller (US PGPub No. 20040100994), Bhattacharya et al (US Patent No. 7,047,385), Berg et al (US Patent No. 6,732,247) and Martin et al (US PGPub No. 20020156995).

For claim 10, the combined teachings of Miller, Bhattacharya and Berg disclose the invention as per rejection of claim 6 above.

These teachings fail to disclose a number of pipeline stages used depends upon an access latency of each bank and a desired throughput rate.

Martin helps disclose the optimal number of stages for maximum throughput is determined by the ratio of the cycle period over the forward latency of a pipeline stage (par. 0115).

It would have been obvious to a person of ordinary skill in the art at the time of the invention to combine Miller, Bhattacharya, Berg and Martin that a number of pipeline stages used depends upon an access latency of each bank and a desired throughput rate because, when fine pipelines are desirable, the number of pipeline stages may be changed in order to achieve desired high-throughput and low latency (par. 0096), as taught by Martin.

8. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Miller (US PGPub No. 20040100994), Bhattacharya et al (US Patent No. 7,047,385), Berg et al (US Patent No. 6,732,247) and Tsuruta et al (US PGPub No. 20030037226).

For claim 11, the combined teachings of Miller, Bhattacharya and Berg disclose the invention as per rejection of claim 6 above.

These teachings fail to disclose a clock frequency and a data path width for the pipeline architecture is determined.

Tsuruta helps disclose a processor architecture comprising a pipeline, shared by each of the program streams, having N pipeline stages operable at a frequency F, an instruction developing section which develops one instruction into Q parallel instructions, and a first mechanism executing one program stream for every M cycles depending on a required operation performance and selectively executing the Q parallel instructions (par. 0018).

It would have been obvious to a person of ordinary skill in the art at the time of the invention to combine Miller, Bhattacharya, Berg and Tsuruta that a clock frequency and data path width for a pipeline may be determined because this would allow for the system to suit a required performance and further reduce power consumption (par. 0018), as taught by Tsuruta.

9. Claims 12-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miller (US PGPub No. 20040100994), Bhattacharya et al (US Patent No. 7,047,385), Berg et al (US Patent No. 6,732,247) and Zahir et al (US Patent No. 6,052,802).

For claim 12, the combined teachings of Miller, Bhattacharya and Berg disclose the invention as per rejection of claim 6 above.

These teachings fail to disclose a number of pipeline stages relates to a number of clock cycles.

Zahir helps disclose a number of computer cycles equal to the number of pipeline stages contained in a computer (col. 1, lines 26-27).

It would have been obvious to a person of ordinary skill in the art at the time of the invention to combine Miller, Bhattacharya, Berg and Zahir to make a number of pipeline stages related to a number of clock cycles because it is common knowledge that a design technique called a pipeline involves the output of one process to serve as input to a second, etc., during which one or more processes occur during a computer clock cycle (col. 1, lines 13-20), as taught by Zahir.

For claim 13, the combined teachings of Miller, Bhattacharya, Berg and Zahir as per rejection of claim 12 further help disclose the number of pipeline stages is the same as the number of clock cycles (col. 1, lines 26-27).

10. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Miller (US PGPub No. 20040100994), Bhattacharya et al (US Patent No. 7,047,385), Berg et al (US Patent No. 6,732,247) and Potter (US Patent No. 6,505,269).

For claim 18, the combined teachings of Miller, Bhattacharya and Berg disclose the invention as per rejection of claim 6 above.

These teachings fail to disclose memory operations from different banks having different memory addresses of one of the systolic memory arrays are interleaved.

Potter helps disclose interleaving occurs between banks and arrays of memory (col. 7, line 45).

It would have been obvious to a person of ordinary skill in the art at the time of the invention to combine Miller, Bhattacharya, Berg and Potter to allow different memory addresses to be interleaved because this arrangement contributes to a streaming mode of operation (col. 7, lines 43-45), as taught by Potter.

Allowable Subject Matter

11. The following is a statement of reasons for the indication of allowable subject matter:

For claim 21, no combination of the aforementioned references describe access latency for a bank is represented by 2i+L, where i represents the time it takes to allow an address to reach a desired i th bank and L represents the cycles of latency to access the memory.

Claims 22-24 are allowable as being, directly or indirectly, dependent on claim 21 and having additional allowable features therein.

For claim 30, no combination of the aforementioned references describe access latency for a bank is represented by 2i+L, where i represents the time it takes to allow

an address to reach a desired i th bank and L represents the cycles of latency to access the memory.

For claim 39, no combination of the aforementioned references describe access latency for one bank of the plurality of separate systolic memory arrays is represented by 2i+L, where i represents the time it takes to allow an address to reach a desired i th bank and L represents the cycles of latency to access the memory.

Citation of Pertinent Prior Art

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Abrosimov et al (US PGPub No. 20030097541) discloses a processing architecture for performing a plurality of tasks compises a conveyor of pipe stages, having a certain width and a clock signal.

Wich (US Patent No. 7,071,748) discloses a charge pump clock for a memory device.

Contact Information

13. Any inquiries concerning this action or earlier actions from the examiner should be directed to Daniel Kim, reachable at 571-272-2742, on Mon-Fri from 10:00am-6:30pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sanjiv Shah, is also reachable at 571-272-4098.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information from published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. All questions regarding access to the Private PAIR system should be directed to the Electronic Business Center (EBC), reachable at 866-217-9197.

DK

9-26-06

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